5723/5724 and 5753/5754
CONTROL INTERFACE DESCRIPTION
(Standard Configuration for use with 57XX-XXXX-2-X Series Modules)

PIN	SIGNAL NAME	DESCRIPTION
1	INHIBIT	3.5 to 30V input to inhibit charger. 10kΩ load impedance (reference Figure 1).
2		NO CONNECTION
3	OVER TEMP STATUS INDICATOR	Internal 1kΩ resistor to +12V. FET output rated at 40V, 100mA. Fault indicated by low condition (reference Figure 2). This is a warning indicator only.
4	PROGRAM RTN/GND	Differential input return for program voltage. Requires no connection if unit is configured as single ended or internal control (reference Figure 3).
5	PROGRAM VOLTAGE	0 to 10V control differential input for 0 to 100% rated output voltage (reference Figure 3). Models 5753 and 5754 require driving two circuits connected in parallel.
6	OVER VOLTAGE STATUS INDICATOR	Internal 1kΩ resistor to +12V. FET output rated at 40V, 100mA. Maximum output voltage can be programmed by an internal 10-turn potentiometer. If this voltage is exceeded a fault will be indicated by a low signal at this pin. The charger will also be inhibited to prevent it from exceeding this voltage. The over-voltage protection potentiometer is accessible at the hole labeled OVP Adjust. Counter-clockwise motion of this potentiometer is required to increase the over-voltage set point (reference Figure 4).
7	V_{OUT} PEAK HOLD	Output which monitors output voltage with a peak hold circuit. 0 to 10V represents 0 to 100% rated output voltage. To ensure good stability, the time constant of this circuit is ☐ 2 min. This should be considered when lowering the operating voltage from a higher value. For a direct reading of the output voltage, pin 8 can be monitored (reference Figure 5).
8	V_{OUT} MONITOR	Output which directly monitors output voltage. 0 to 10V represents 0 to 100% rated output voltage (reference Figure 6).
9	+12VDC	12V output capable of delivering 30mA (reference Figure 7).
10		NO CONNECTION
11	+10VDC REFERENCE	10V output capable of delivering 2mA (reference Figure 8).
12	SIGNAL RTN	Signal return for any external control circuitry. Common to pin 14.
13	END OF CHARGE INDICATOR	Internal 1kΩ resistor to +12V. FET output rated at 40V, 100mA. When PFN is charged to programmed voltage the output is pulled low (reference Figure 9).
14	SIGNAL RTN	Signal return for any external control circuitry. Common to pin 12.
15	GND INTERLOCK	Must be connected to signal return pin or charger will remain inhibited (reference Figure 10).

NOTE: The Program Voltage input can be optionally configured for 0 - 10V single-ended, 0 - 5V differential or single ended, or internal control via a 10-turn potentiometer. This potentiometer is accessible at the hole labeled HV Adjust and clockwise motion of this potentiometer causes an increase in the output voltage. Similarly, the V_{OUT} Peak Hold and the V_{OUT} Monitor can be optionally scaled to provide 0 - 5V full-scale signal levels. Any of these options must be configured at the factory and specified at time of order.

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5723/5724/5753/5754 INTERFACE CIRCUITS

FIG. 1 INHIBIT

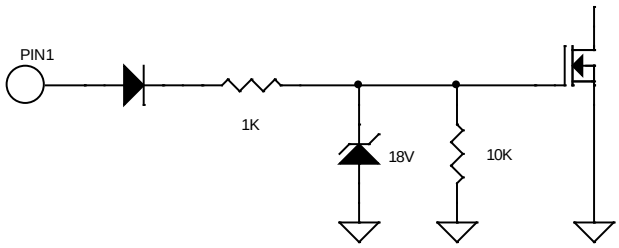


FIG. 2 OVER TEMP STATUS

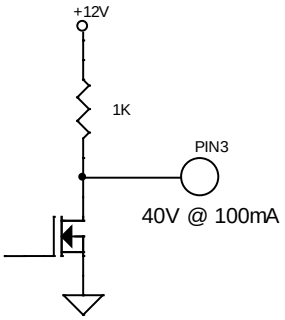
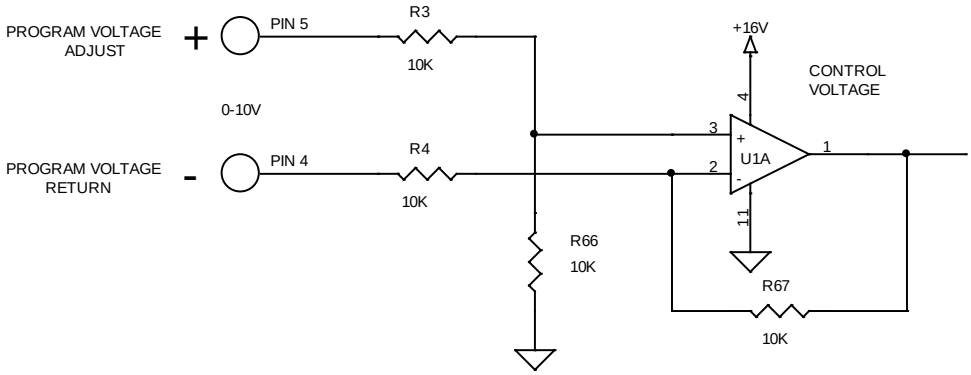
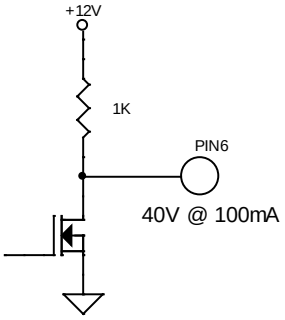


FIG. 3 PROGRAM VOLTAGE



0-10V CONTROL R66,67 = 10K
0-5V CONTROL R66,67 = 20K

FIG. 4 OVER VOLTAGE STATUS



4813C.DSN

FIG. 5 VOLTAGE PEAKHOLD

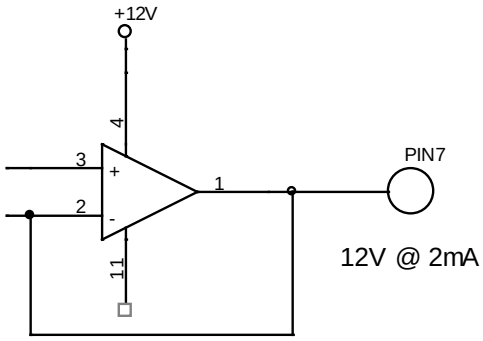


FIG. 6 VOLTAGE MONITOR

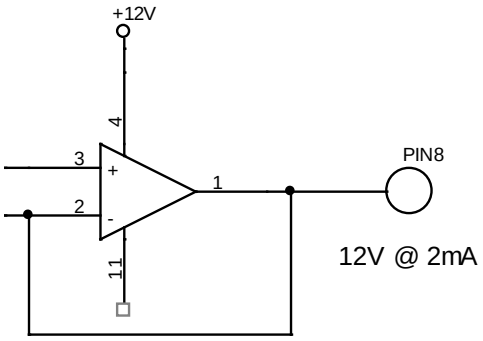
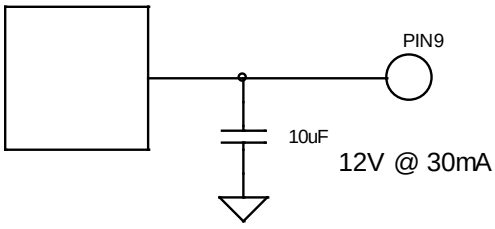


FIG.7 +12VDC



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5723/5724/5753/5754 INTERFACE CIRCUITS

FIG. 8 +10VDC REFERENCE

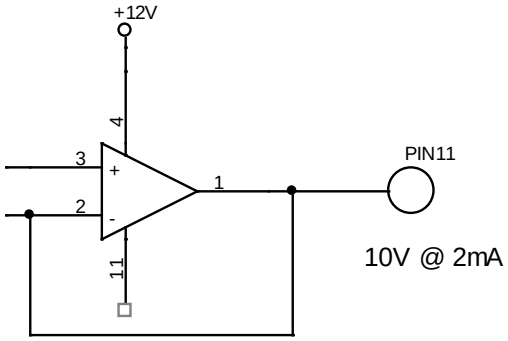

FIG.9 END OF CHARGE

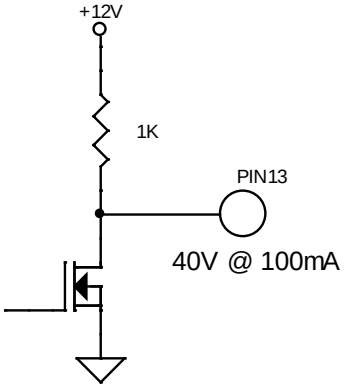

FIG.10 GND INTERLOCK